Exhibit 5

[redacted]

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Paper 13
Entered: December 12, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00847
Patent 10,268,608 B2

Before JON M. JURGOVAN, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–12 of U.S. Patent No. 10,268,608 B2 (Ex. 1001, "the '608 patent"), along with the Declaration of Dr. Robert Wedig. Paper 1 ("Pet."); Ex. 1003. Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). In the Preliminary Response, Patent Owner indicates that it filed a statutory disclaimer disclaiming claims 6–12 of the '608 patent. Prelim. Resp. 2–3 (citing Ex. 2001). With authorization, Petitioner filed a Reply (Paper 9, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 10, "PO Sur-reply").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). Upon consideration of the Petition, the Preliminary Response, Petitioner's Reply, and Patent Owner's Sur-reply, along with the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the '608 patent. Accordingly, for the reasons that follow, we institute an *inter partes* review of claims 1–5 of the '608 patent.

A. Related Matters

The parties indicate this Petition is related to the following district court litigations:

Netlist, Inc. v. Micron Technology, Inc., No. 1:22-cv-00136 (W.D. Tex.);

Netlist, Inc. v. Samsung Electronics Co., Ltd., No. 2:22-cv-00293 (E.D. Tex.);

Netlist, Inc. v. Micron Technology, Inc., No. 2:22-cv-00203 (E.D. Tex.);

Netlist, Inc. v. Samsung Electronics Co., Ltd., No. 2:21-cv-00463 (E.D. Tex.).

Paper 12, 1; Paper 3, 1.

The parties also indicate this Petition is related to the following Board proceedings:

Micron Technology, Inc. v. Netlist, Inc., IPR2023-00205;

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711;

Micron Technology, Inc. v. Netlist, Inc., IPR2022-00237 ("the Micron '237 IPR");

Micron Technology, Inc. v. Netlist, Inc., IPR2022-00236; and

SK hynix Inc. v. Netlist, Inc., IPR2017-00730.

Paper 12, 1–2; Paper 3, 1.

Further, the parties indicate this Petition is related to the following applications:

U.S. Patent Application No. 18/452,554; and

U.S. Patent Application No. 17/114,478.

Paper 12, 2; Paper 3, 2.

B. The '608 Patent

The '608 patent, titled "Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers," relates to a memory system which controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 2:43–45, 4:65–66.

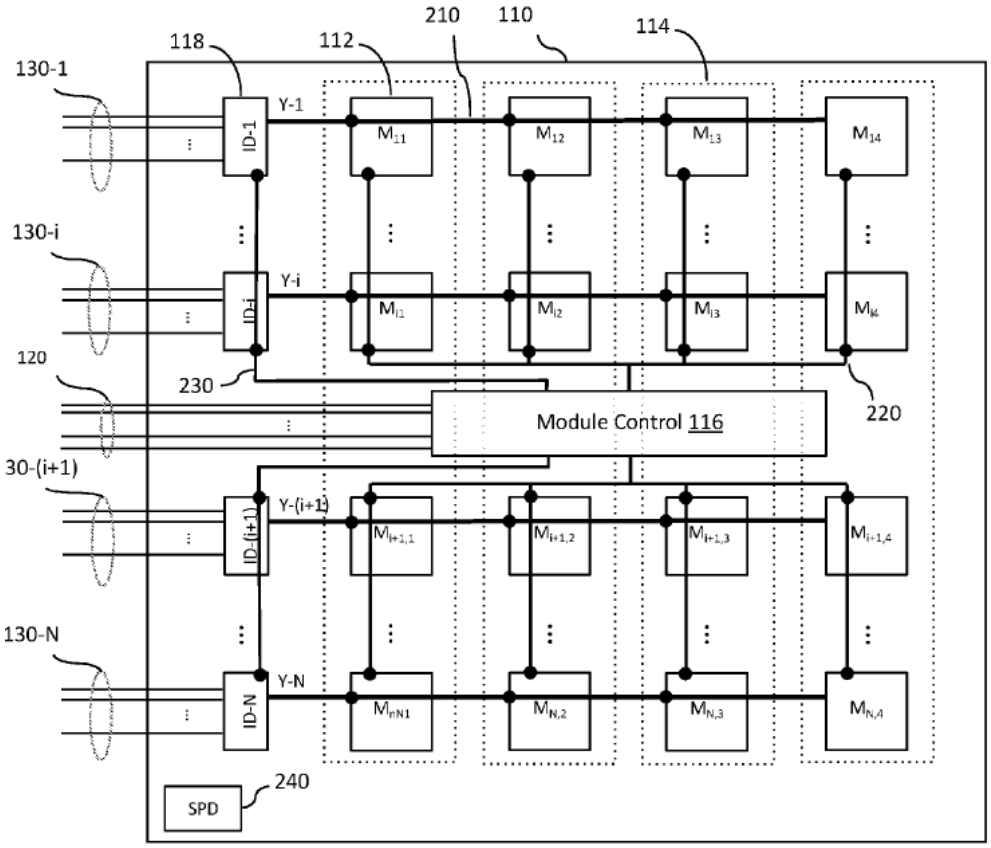

FIG. 2A

As shown in Figure 2A, above, memory module 110 includes module control device 116 and a plurality of memory devices 112. Ex. 1001, 4:65–66, 6:4–5. Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller (MCH) (not shown). *Id.* at 4:20–23, 4:65–5:4. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation devices, or buffers, 118, that is, the group of data/strobe signal lines 130-1 is coupled to isolation device ID-1, for example. *Id.* at 4:23–25; *see id.* at 6:20–25. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:17–20, 6:30–32. As an example, along the top of memory module 110 shows isolation device ID-1 "is associated with [a] first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and is coupled between the group

of system data/strobe signal lines 130-1 and the first group of memory devices" via module data/strobe lines 210. *Id.* at 6:20–25.

In operation, memory module 110 "perform[s] memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.)." Ex. 1001, 3:29–32. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:32–34, 4:66–5:3. For example, "[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118." *Id.* at 7:63–66. And "read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130." *Id.* at 7:66–8:3.

As can be seen in Figure 2A, and as the '608 patent explains, there are "unbalanced" lengths of control wires to respective memory devices which causes a "variation of the timing" of signals due to the variation in wire length. *See* Ex. 1001, 2:20–31; *see also id.* at 8:22–55. To account for timing issues, each isolation device, or data buffer, 118 is "responsible for providing a correct data timing" and "providing the correct control signal timing." *Id.* at 8:56–9:3. In particular, "isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation." *Id.* at 15:23–26. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information which is used to "properly time transmission" of a later-read operation. *Id.* at 15:45–50.

C. Challenged Claims

Petitioner challenges claims 1–12 of the '608 patent in the Petition. Pet. 1.

Subsequent to the filing of the Petition, Patent Owner filed a statutory disclaimer under 35 U.S.C. § 253(a) to disclaim claims 6–12 of the '608 patent. Ex. 2001 ("Disclaimer in a Patent Under 37 C.F.R. 1.321(a);" Electronic Payment Receipt;" "Electronic Acknowledgment Receipt"); *see* 35 U.S.C. § 253(a); 37 C.F.R. § 1.321(a). Because Patent Owner's statutory disclaimer satisfies all regulatory requirements to disclaim claims 6–12, we do not consider Petitioner's challenges to those claims. *See* Ex. 2001; 37 C.F.R. § 1.321(a); *General Electric Co. v. United Techs. Corp.*, IPR2017-00491, Paper 9 (PTAB July 6, 2017) (precedential).

Claim 1 is the only independent claim. Claim 1, which is illustrative, is reproduced below, with bracketed letters provided by Petitioner (*see* Pet. xiii) added to limitations for reference purposes.

> 1. [pre] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal[1] lines, the memory module comprising:
>
> [a] a module board having edge connections for coupling to respective signal lines in the memory bus;
>
> [b] a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being

[1] Data signals lines are referred to as "DQ" signal lines, and data strobe lines are referred to as "DQS" signal lines. *See* Ex. 1001, 10:31–35.

> further configured to receive a system clock signal and output a module clock signal; and
>
> [c] memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
>
> [d] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, [e] wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, [f] wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Ex. 1001, 19:14–55.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–5 are of the '608 patent are unpatentable based on the following grounds[2]:

[2] Because Patent Owner has disclaimed claims 6–12 of the '608 patent, we do not further address these claims, or associated grounds, because they are no longer at issue in this proceeding.

Ground	Claim(s) Challenged	35 U.S.C §	Reference(s)/Basis
1	1–5	103(a)[3]	Hiraishi[4], Butt[5]
2	1–5	103(a)	Ground 1, Tokuhiro[6]
3	5	103(a)	Ground 1 or 2, Ellsberry[7]

Pet. 1.

III. DISCRETIONARY DENIAL

Institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech, Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) ("[T]he PTO is permitted, but never compelled, to institute an IPR proceeding."); 35 U.S.C. § 314(a). Pursuant to 35 U.S.C. § 325(d), in determining whether to institute an *inter partes* review, "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." In evaluating arguments under § 325(d), we use

> [a] two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

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[3] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. § 103, and was effective on March 16, 2013. Because the '608 patent claims priority before the effective date of the applicable AIA amendments (*see* Ex. 1001, code (60)), we refer to the pre-AIA version of 35 U.S.C. § 103.
[4] US 2010/0312956 A1, published December 9, 2010 (Ex. 1005, "Hiraishi").
[5] US 2007/0009791 A1, published January 11, 2007 (Ex. 1029, "Butt").
[6] US 8,020,022 B2, issued September 13, 2011 (Ex. 1006, "Tokuhiro").
[7] US 2006/0277355 A1, published December 7, 2006 (Ex. 1007, "Ellsberry").

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"); *see also Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph) (listing factors to consider in evaluating the applicability of § 325(d)) ("*Becton Dickinson*").

Patent Owner contends that we should deny the Petition under § 325(d) because Petitioner relies on the same or substantially the same art and arguments as previously presented to the Board in the Micron '237 IPR, and because Petitioner has not demonstrated the Board materially erred in denying institution in the Micron '237 IPR. *See* Prelim. Resp. 3–25.

In particular, Patent Owner argues that the Hiraishi reference is essentially the same as the Osanai reference asserted in the Micron '237 IPR. Prelim. Resp. 5. Patent Owner also argues that the Butt reference is not substantively relied upon by Petitioner, and serves only as evidence of what a person of ordinary skill in the art would have understood about Hiraishi's disclosure. *See id.* 5–12. For example, Patent Owner argues that "Petitioner does not assert that Butt teaches a data path that includes a delay circuit, the element that the Board found to be missing from Osanai/Hiraishi" in the Micron '237 IPR. *Id.* at 6. Rather, Patent Owner argues, "the Petitioner relies exclusively on Hirashi's original and unmodified S4 write and read leveling operations to satisfy the Element [1f] limitation of a 'delay circuit configured to delay a [signal] through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.'" *Id.* at 9 (second alteration added). Patent Owner also contends that Tokuhiro, which is also asserted in this case, is the same as the Tokuhiro reference that was already considered in the Micron

'237 IPR. *Id.* at 12. Patent Owner further asserts that Ellsberry is relied upon only in the alternative to the showing provided in the first ground under Hiraishi's teachings, and Ellsberry therefore is cumulative to what has been presented in the Micron '237 IPR. *Id.* at 12–13.

Petitioner concedes that Hiraishi is essentially the same as Osanai, but emphasizes that the institution decision in the Micron '237 IPR was based on anticipation, rather than obviousness, as is the case here. Pet. Reply 1. Petitioner draws the Board's attention to *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00711 ("the Samsung '711 IPR") and *Micron Technology, Inc. v. Netlist, Inc.*, IPR2022-00236 ("the Micron '236 IPR"), "where Institution was granted for similar claims based on *obviousness* grounds similar to those here (i.e., Hiraishi/Osanai in view of Butt and/or Tokuhiro)." *Id.* According to Petitioner, "§ 325(d) and Part 1 of *Advanced Bionics* favor Petitioner, because Petitioner . . . presents 'the same or substantially the same prior art or arguments' that were *accepted* by the Board in IPR2022-00236 and -00711." *Id.* at 2.

Further, Petitioner argues that "Butt (which was not considered in IPR2022-00237) is an integral part of Ground 1." Pet. Reply 2. Petitioner asserts, with respect to a data path that includes a delay circuit, that "[h]ere, the Petition shows how those limitations are obvious . . . similar to the showings that were accepted by the Board in Micron's IPR2022-00236 and Samsung's IPR2022-00711." *Id.* at 3; *see also* Pet. 113–114 (citing Ex. 1041, 18–19, n.2) ("[T]his combination clearly renders obvious 'a data path' with a 'delay circuit,' which Micron's '608 petition [in the Micron '237 IPR] failed to show."). Petitioner also asserts that the Board never reached the consideration of Tokuhiro in the Micron '237 IPR because it found that Tokuhiro was not relied upon for a deficiency of the teaching of a

claim limitation under the Board's consideration of anticipation by Osanai only, which was dispositive. *Id*. at 1–2.

In response to Petitioner's arguments, Patent Owner asserts that "§ 325(d) is a tool to conserve Board resources and prevent patent owner harassment, not a mechanism for a petition to piggyback off of other proceedings involving different patents." PO Sur-reply 1. Further, Patent Owner argues that the claims at issue in the Micron '236 IPR are materially different than those at issue in this proceeding. *Id.* at 2. Specifically, Patent Owner asserts that "the claims in Micron -0236 do not include a 'delay circuit' of any kind, least of all one which 'delay[s] a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.'" *Id.*

Under *Advanced Bionics*, *Becton Dickinson* factors (a), (b), and (d) are considered in the evaluation of whether the same or substantially the same art or arguments were previously presented to the Office and factors (c), (e), and (f) relate to the second part (i.e., "whether the petitioner has demonstrated a material error by the Office" in its prior consideration of the prior art or arguments). *Advanced Bionics*, 10.

We first consider "whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office." *Advanced Bionics*, 8. Considering the first factor, that is, whether the same or similar art was before the Office, Patent Owner asserts, and Petitioner does not dispute, that the Hiraishi reference is essentially the same as the Osanai reference asserted in the Micron '237 IPR. We agree. As to the asserted secondary reference, Butt, we have reviewed the Petition and we agree with Patent Owner that although Butt is a named secondary reference, Hiraishi is

the main reference relied upon for the teachings of the claim limitations, and Butt is used to provide further explanations or interpretations of the teachings of Hiraishi and/or to explain the knowledge of one of ordinary skill in the art. *See* Pet. 15–53. As for Tokuhiro, although that reference was not reached in the Micron '237 IPR, it was nonetheless art that was before the Board in that proceeding. Thus, substantially the same prior art was previously before the Board. Accordingly, we find that the first part of the *Advanced Bionics* test applies.[8]

As to the second part of the *Advanced Bionics* test, we consider Petitioner's argument that in the Micron '237 IPR Osanai was previously considered as an anticipatory reference, whereas here the similar reference, Hiraishi, is used in an obviousness challenge. *See* Pet. Reply 1. Patent Owner contends that there was no error made by the Board in the Micron '237 IPR. Prelim. Resp. 23–24.

We are persuaded that because of the facts here—an obviousness challenge asserted in this Petition and an anticipation challenge[9] in the Micron '237 IPR—that the contentions here were not previously considered by the Board. Although Patent Owner argues that the contentions in the instant Petition and the Micron '237 IPR are substantially the same (Prelim. Resp. 23), we do not agree because the argument and evidence here is being viewed in light of an obviousness standard rather than that of an anticipation standard and Petitioner has provided additional argument and evidence that

[8] We agree with Patent Owner that the first part of § 325(d) requires either that the same or substantially the same art previously was presented to the Office *or* the same arguments be previously presented. PO Sur-reply 4–5.
[9] The evaluation of the anticipation challenge in the Micron '237 IPR was dispositive in determining the outcome of the decision on institution on all grounds. *See* Ex. 1041, 14–21.

is not in the Micron '237 IPR petition, including Butt's support for the knowledge of one of ordinary skill. Moreover, as we discuss below in the merits of the instant Petition, we have preliminarily determined that Petitioner's showing of the data path and delay circuit configured to delay a signal through the data path are sufficiently demonstrated as taught or suggested in the obviousness challenge, unlike the anticipation showing in the Micron '237 IPR. *See* Ex. 1041, 17–20. So, in other words, while Patent Owner's argument that there was no error made by the Board in the Micron '237 IPR may be meritorious, the operative issue is, however, that different obviousness-based arguments are being made here. In the Micron '237 IPR the Board was limited to the arguments presented in that prior petition. *See, e.g., Sirona Dental Sys. GmbH v. Institut Straumann AG*, 892 F.3d 1349, 1356 (Fed. Cir. 2018) ("It would . . . not be proper for the Board to deviate from the grounds in the petition and raise its own obviousness theory . . . .").

Under these particular circumstances, the Board did not have the opportunity in the previous Micron '237 IPR to evaluate the challenged claims based on obviousness over Hiraishi and Butt. With this, Patent Owner's argument that there was no error in the Micron '237 IPR is not relevant to the circumstances here, nor do we find that Petitioner was required to explain why the Board erred in its institution decision in the Micron '237 IPR. And considering the *Becton Dickinson* factors for the second part of the inquiry under the *Advanced Bionics* framework[10], factors

[10] *Becton Dickinson* factors include:

> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; . . .

(c) and (e) do not apply given that the Board previously considered a different challenge, and factor (f) favors that we do not discretionarily deny because new arguments and evidence on a new legal basis are raised in this proceeding. Thus, consideration of these factors favors that we do not exercise our discretion to deny institution.

Accordingly, we decline to exercise our discretion to deny institution.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Wedig, Petitioner proposes that a person of ordinary skill in the art at the time of invention of the '608 patent "would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field." Pet. 2 (citing Ex. 1003 ¶ 37). Petitioner further proposes that a skilled artisan "would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers," and "would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other components of a memory system,

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(e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
(f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton Dickinson, 17–18.

including sophisticated circuits such as ASICs and CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers." *Id.* at 2–3 (citing Ex. 1003 ¶ 37).

Patent Owner presents no proposed qualifications. *See* Prelim. Resp.

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citation omitted). The level of ordinary skill in the art is also reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). For purposes of this Decision and with the exception of the qualifier "at least" with respect to experience which renders the level of ordinary skill in the art ambiguous and may encompass levels beyond ordinary, we adopt the assessment offered by Petitioner, as it is consistent with the '608 patent and the asserted prior art.

B. Claim Construction

In this *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claims in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2021). Under the principles set forth by our reviewing court, the "words of a claim 'are generally given their ordinary and customary meaning,'" as would be understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "In determining the meaning of the disputed claim

limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner asserts that "the Board need not expressly construe any claim term because the prior art invalidates the claims under any plausible construction, in accordance with 37 C.F.R. §42.100(b)," but offers references to portions of the '608 patent as examples of usage of certain claim terms. Pet. 7.

Patent Owner does not present any proposed claim constructions. *See* Prelim. Resp.

We determine that we need not expressly construe any claim terms to resolve the parties' disputes on the current record. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.,* 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103 if "the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective date of the claimed invention to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103 (2011); *see also KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations

including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective indicia of nonobviousness.[11] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Asserted Obviousness of Claims 1–5 Over Hiraishi and Butt

Petitioner contends that claims 1–5 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Hiraishi and Butt. Pet. 15–59. In support, Petitioner also relies upon the Wedig Declaration. Ex. 1003.

We begin our discussion with brief summaries of Hiraishi and Butt, and then address the evidence and arguments presented.

1. Hiraishi (Ex. 1005)

Hiraishi relates to a memory module having memory chips and data register buffers arranged in a manner which allows for a high data transfer rate. Ex. 1005, code (57). Figure 1, reproduced below, "is a schematic diagram of a configuration of a memory module." *Id.* ¶ 13.

[11] No evidence of objective indicia of nonobviousness is presented in Patent Owner's Preliminary Response. *See* Prelim. Resp.

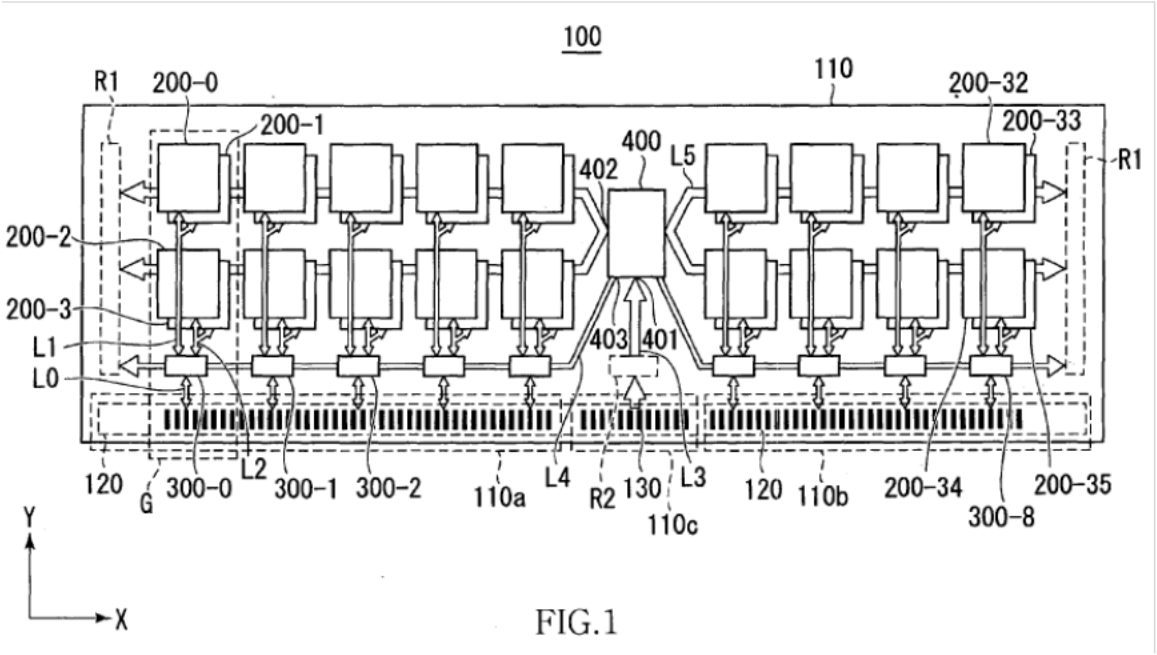

FIG.1

As shown in Figure 1, memory module 100 includes a plurality of memory chips 200 mounted on module substrate 110. Ex. 1005 ¶ 45. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and command/address/control register buffer 400. *Id.* ¶ 46. Still further, memory module 100 includes "data connectors 120 [which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller" electrically connected to the connectors. *Id.* ¶¶ 47–48 (memory controller not shown).

As can be seen in Figure 1, and as further detailed in Figure 7, "data register buffer 300 intervenes between the data connectors 120 and the memory chips 200." Ex. 1005 ¶ 103. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 19.

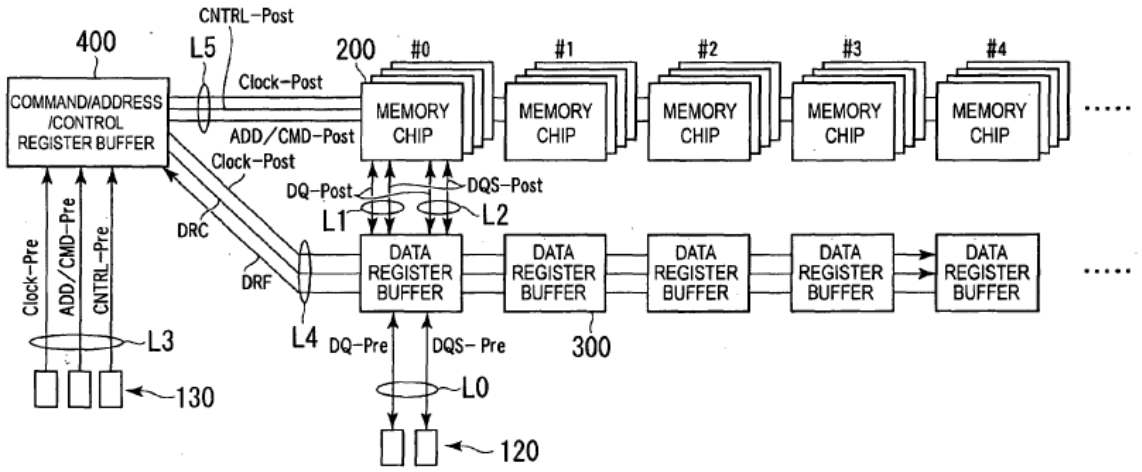

FIG.7

As shown in Figure 7, above, "data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2." Ex. 1005 ¶ 103. "[A] plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post."[12] *Id.* In addition, "a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post." *Id.*

Further, "[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post."

[12] Similar to the '608 patent, in Hiraishi, "DQ" refers to a data signal and "DQS" refers to a data strobe signal (*see* Ex. 1005 ¶ 91), and in Hiraishi, "DQ-Pre" refers to data signals input to Data Buffer Register Buffer and "DQ-Post" refers to data signal output from Data Buffer Register (*id.* ¶ 107, Fig. 7).

Ex. 1005 ¶ 104. As such, "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller." *Id.* Hiraishi "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal" via leveling operations. *Id.* ¶ 140. The write leveling and read leveling operations are provided via write leveling and read leveling circuits in the data register buffer, as shown in Figure 5, which is a block diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 83.

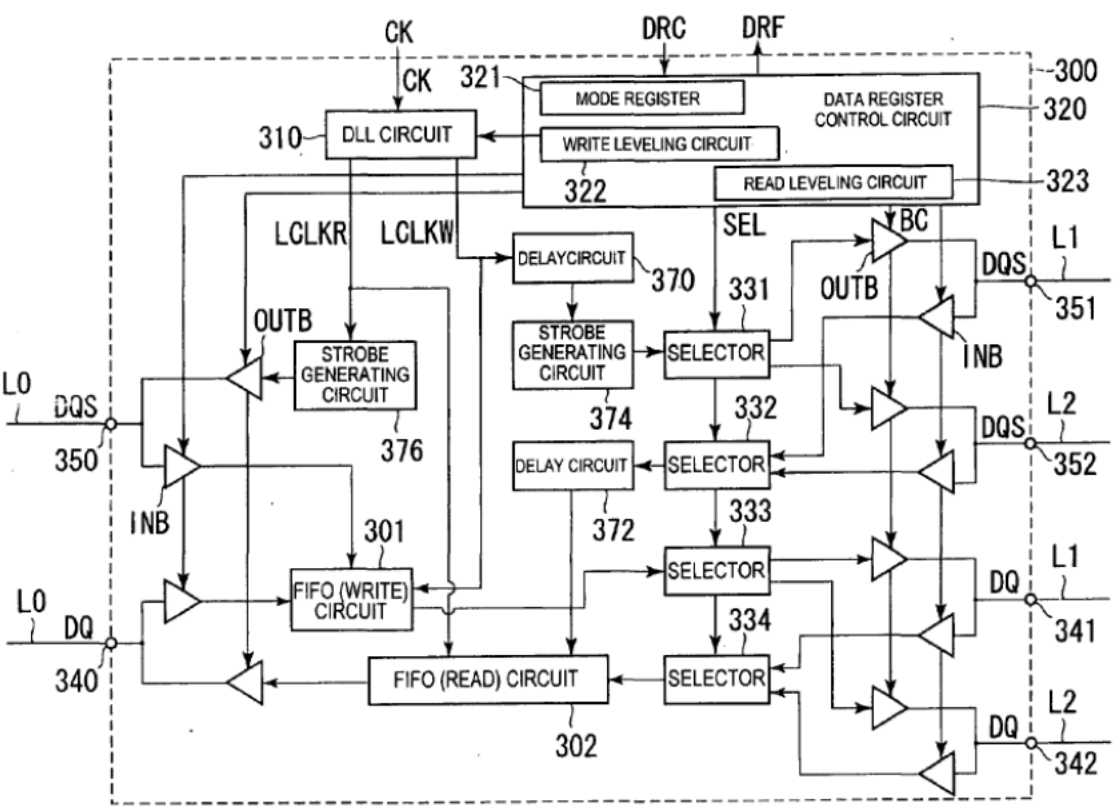

FIG.5

As shown in Figure 5, above, data register buffer 300 includes a data register control circuit 320 having write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶ 90. The write leveling and read leveling operations "adjust a write timing or a read timing in consideration of a propagation time of a

signal." *Id.* ¶ 140. For example, in a write operation, "[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side." *Id.* ¶ 143. To compensate for that, "write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS." *Id.* ¶ 145. An exemplary read leveling operation also adjusts signal timing for a read operation. *See id.* at ¶¶ 147–151.

2. Butt (Ex. 1029)

Butt relates to DQS strobe centering in memory systems such as DDR [double data rate] memories. Ex. 1029 ¶¶ 2–3. Specifically, Butt describes calibrating a data valid window by setting a base delay for one or more datapaths to a predetermined value, determining an optimum offset delay value for each data path based on actual memory access, and delaying a read data strobe signal based on both the base delay and optimum offset delay for each datapath. *Id.* ¶ 5. Butt's Figure 2, reproduced below, shows a detailed block diagram of a circuit that may serve as a memory interface between a memory controller and a memory. *See id.* ¶¶ 15–17.

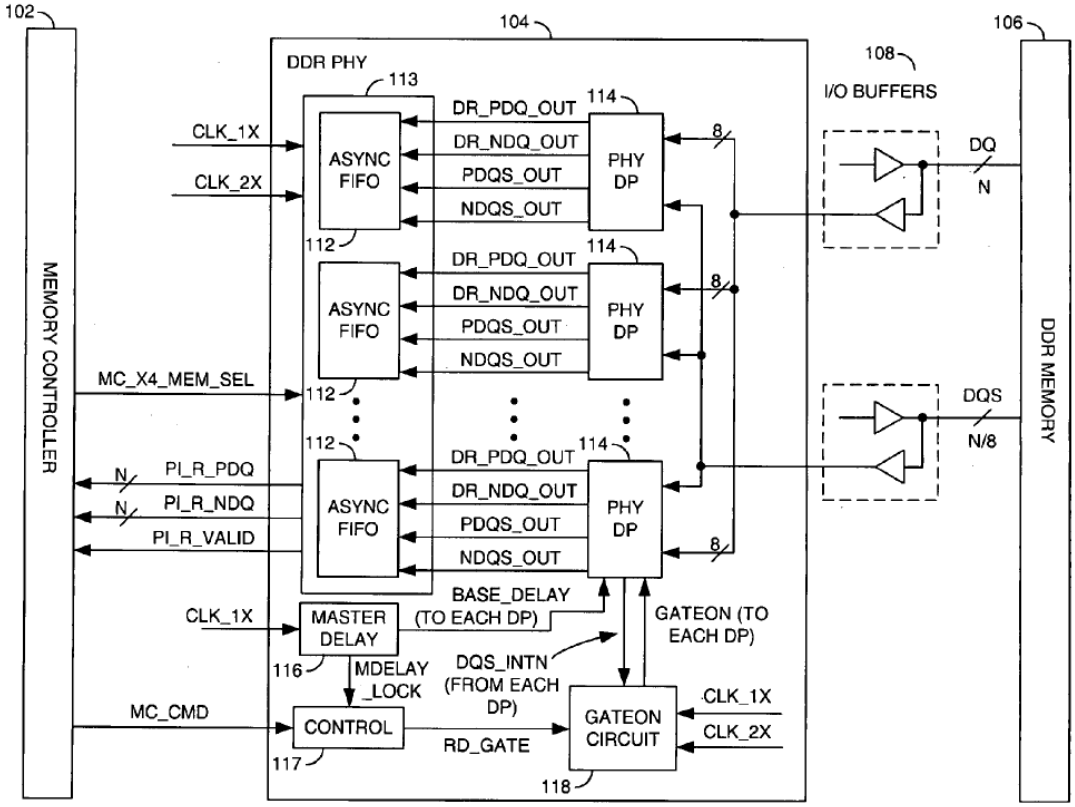

FIG. 2

As shown in Figure 2, above, circuit 104 comprises a number of physical read datapaths 114 that "may be configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal of signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal . . . from the programmable gating signal generator 118." Ex. 1029 ¶ 17. "[A]synchronous FIFOs 112 may be configured to interface the physical read datapaths 114 with the memory controller 102." *Id.* In operation, "the read datapaths 114 are generally programmable from when the data/strobe pairs DQ/DQS are received at the input to the circuit 104, to sampling the

read data with the read data strobe signal DQS, and passing the data to the memory controller 102." *Id.* ¶ 20.

3. Discussion

a. Claim 1

i. Preamble

Petitioner asserts that Hiraishi discloses "[m]emory module 100 is operable to communicate with the memory controller (MCH 12) via a memory bus (line 23) that is coupled to data line L0 and the command/address/control line L3 . . . on the memory module 100." Pet. 16 (citing Ex. 1003 ¶ 116; Ex. 1005 ¶¶ 65, 69, Figs. 2, 3). In particular, Petitioner asserts that Hiraishi discloses "memory bus (line 23) includes a set of control/address signal lines coupling, through connectors 130 . . . to command/address/control line L3, and multiple sets of data/strobe signal lines, each set coupling, through connectors 120 . . . to data line L0." *Id.* (citing Ex. 1003 ¶ 117; Ex. 1005 ¶¶ 47, 49, 69, 102–103, Figs. 1, 7).

At this stage, Patent Owner presents no arguments specifically related to the preamble. *See generally* Prelim. Resp.

We have reviewed the evidence and argument, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that Hiraishi teaches the preamble of claim 1.

ii. Limitation 1[a]

Petitioner asserts that Hiraishi's "memory module 100 includes a 'module substrate 110 [which] is a printed circuit board' (PCB) having '*edge connections*' 120 and 130 at its edge for coupling to respective signal lines

in the memory bus connected to the memory controller." Pet. 18 (citing Ex. 1003 ¶ 119–121; citing Ex. 1005 ¶ 45–49).

At this stage, Patent Owner presents no arguments specifically related to limitation 1[a]. *See generally* Prelim. Resp.

We have reviewed the evidence and argument, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that Hiraishi teaches limitation 1[a].

iii. Limitation 1[b]

Petitioner asserts that Hiraishi discloses a module control device, namely, element 400 shown in Hiraishi's Figures 1, 6, and 7 that is mounted on substrate 110. Pet. 19–22 (citing Ex. 1003 ¶¶ 122–123; Ex. 1005 ¶ 59, Fig. 1). Hiraishi refers to element 400 as "a command/address/control register buffer." Ex. 1005 ¶ 45. Petitioner contends that buffer 400 receives system command signals for memory operations "through command/address/control connectors 130 and command/address/control line L3 (Fig. 7) at input terminal 401 (Fig. 6)." Pet. 20–22 (citing Ex. 1003 ¶ 124; Ex. 1005 ¶¶ 18–19, Figs. 6, 7). Petitioner further contends that buffer 400 outputs module command signals, i.e., "ADD/CMD-Post in module command/address/control line L5 (Fig. 7) at output terminal 402 (Fig. 6)," and module control signals, i.e., "DRC . . . on control line L4 (Fig. 7) at output terminal 403 (Fig. 6)," in response to the received system command signals. *Id.* Petitioner also asserts that Hiraishi discloses buffer 400 receives a system clock signal and outputs a module clock signal. *Id.* Specifically, Petitioner identifies "Clock-Pre in L3" and "Clock-Post in L4 and L5." *Id.*

At this stage, Patent Owner presents no arguments specifically related to limitation 1[b]. *See generally* Prelim. Resp.

We have reviewed the evidence and argument, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that Hiraishi teaches limitation 1[b].

iv. Limitation 1[c]

Petitioner asserts that Hiraishi discloses memory devices, specifically, elements 200-0 through 200-35, mounted on a module board that receive module command signals, i.e., "on module command/address/control line L5," and a module clock signal, i.e., "Clock-Post, L5." Pet. 25–27 (citing Ex. 1003 ¶ 130; Ex. 1005, Fig. 1, Fig. 7). Petitioner notes that Hiraishi refers to elements 200-0 through 200-35 as "memory chips." *See id.* at 27–28 (citing Ex. 1005 ¶ 45; Ex. 1003 ¶ 133). Petitioner argues that memory chips 200 perform memory operations in response to module control signals because, for example, "a read or write operation[] is performed in response to 'ACT' and 'Read' or 'Write' command issued by command/address/control register buffer 400." *Id.* at 27 (citing Ex. 1003 ¶ 132; Ex. 1005 ¶¶ 122–136, 163, 170, Figs. 11, 12; Ex. 1020, 33, 56–76). Further, Petitioner asserts that Hiraishi's memory chips are organized into multiple sets of memory devices corresponding to respective sets of data/strobe signal lines. *Id.* at 28 (citing Ex. 1003 ¶ 133). For example. Petitioner contends that one of ordinary skill in the art would have understood that memory chips 200-0 through 200-3 are one set of memory devices that corresponds to data/strobe signal line L0, where signal line L0 is a set of signal lines comprised of DQ-pre and DQS-pre. *Id.*

At this stage, Patent Owner presents no arguments specifically related to limitation 1[c]. *See generally* Prelim. Resp.

We have reviewed the evidence and argument, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that Hiraishi teaches limitation 1[c].

v. Limitation 1[d]

Petitioner asserts that Hiraishi discloses a plurality of buffer circuits, namely, "data register buffer circuits 300-0 to 300-8," corresponding to respective sets of data/strobe signal lines, i.e., "data/strobe signal DQ-Pre and DQS-Pre in L0." Pet. 28–29 (citing Ex. 1003 ¶¶ 135–136; Ex. 1005 ¶¶ 17, 45, 55–56, 84, Fig. 5).

At this stage, Patent Owner presents no arguments specifically related to limitation 1[d]. *See generally* Prelim. Resp.

We have reviewed the evidence and argument, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that Hiraishi teaches limitation 1[d].

vi. Limitation 1[e]

Petitioner asserts that Hiraishi discloses each buffer circuit mounted on the module board and coupled between the respective set of data/strobe signal lines and respective set of memory devices, where each buffer circuit is configured to receive the module control signals and the module clock signal. Pet. 31–33 (citing Ex. 1003 ¶¶ 138–141; Ex. 1005 ¶¶ 45, 55–56, 58, 84–85, 87–88, 103, Figs. 1, 5, 7).

Petitioner contends that the combination of Hiraishi and Butt discloses each buffer circuit includes a data path corresponding to each data signal line in the respective set of data/strobe signal lines. Pet. 33. In particular, Petitioner relies on the annotated versions of Hiraishi's Figure 5, reproduced

below, with orange highlighting to show alleged data paths for respective read and write operations. *Id.*

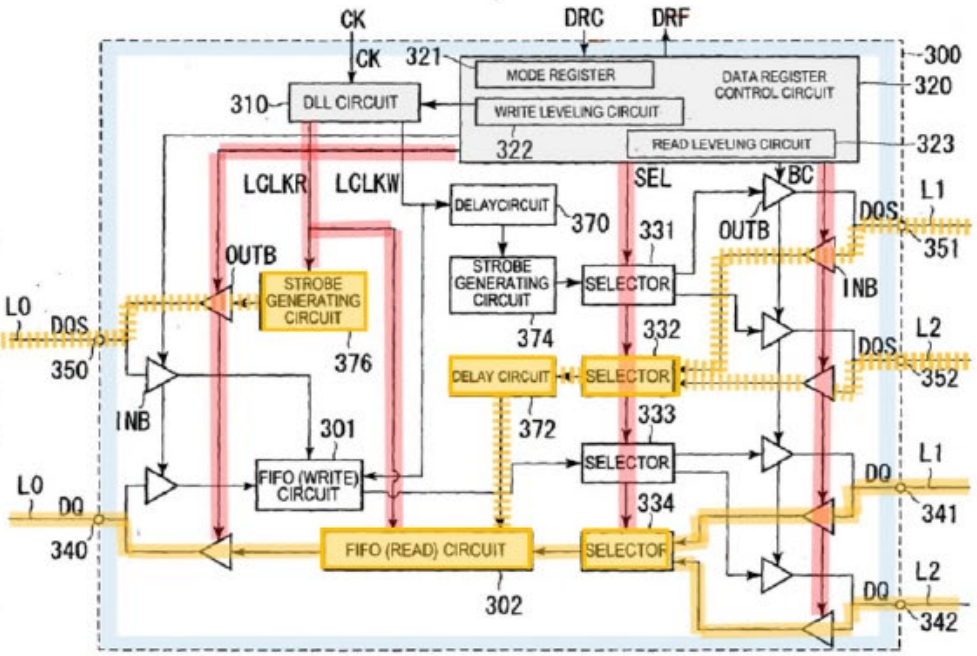

FIG.5

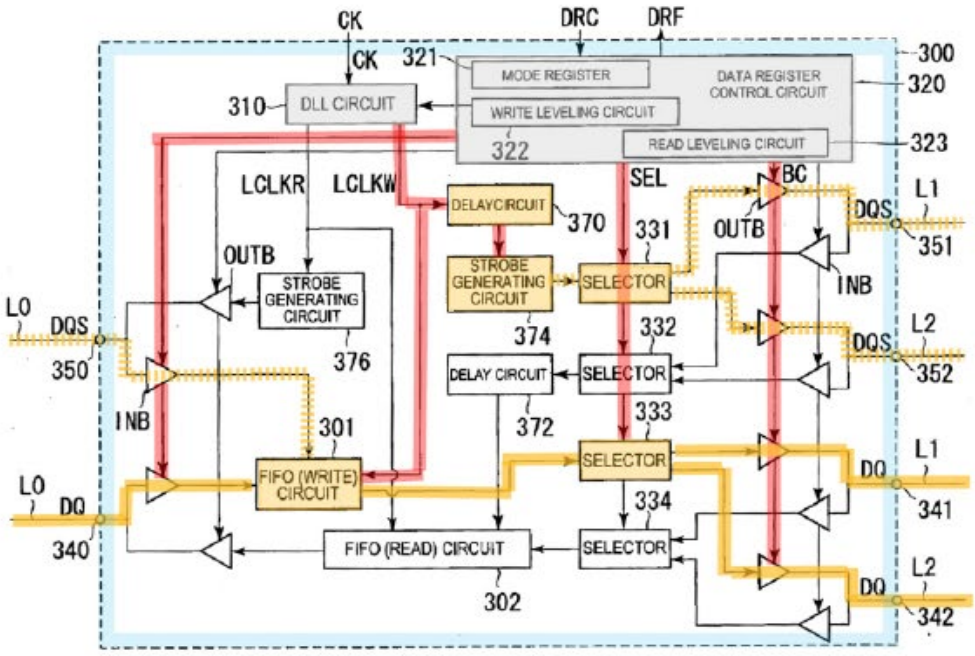

FIG.5

Pet. 34. Petitioner's annotated Figure 5 of Hiraishi, above, depicts the elements and of a data register buffer showing Petitioner's alleged data path for read and write operations. *Id.* Specifically, Petitioner argues that "during memory read or write operations, each respective buffer circuit buffers the data in respective FIFO Read or Write circuits between the data/strobe terminals 340/350 on the left of Figure 5 and the data/strobe terminals 341/342 and 351/352 on the right in Figure 5." *Id.* at 35 (citing Ex. 1003 ¶ 143; Ex. 1005 ¶ 84). Dr. Wedig provides supporting testimony (Ex. 1003 ¶ 142), and refers to Hiraishi's disclosure that:

> As shown in FIG. 5, the data register buffer 300 includes a FIFO (Write) circuit 301 and a FIFO (Read) circuit 302. The FIFO (Write) circuit 301 buffers data DQ that is supplied via an input/output terminal 340 with a data strobe signal DQS that is supplied via an input/output terminal 350. The FIFO (Read) circuit 302 buffers data DQ that is supplied via an input/output terminal 341 or 342 with a data strobe signal DQS that is supplied via an input/output terminal 351 or 352. A strobe generating circuit 376 generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310. A strobe generating circuit 374 generates a data strobe signal DQS to be supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310.

Ex. 1005 ¶ 84 (quoted in Ex. 1003 ¶ 142 (emphasis omitted)).

Petitioner also identifies alleged data paths in Butt, arguing that, "[s]imilarly, Butt discloses that a circuit between a memory controller and DDR memory devices uses strobe signals to sample the data signals and buffers the data samples in FIFOs," and that "such a circuit is an implementation of a 'data path.'" Pet. 35–36 (citing Ex. 1003 ¶ 144; Ex. 1029 ¶ 17, Figs. 2, 3A). Petitioner refers to Figures 2 and 3A of Butt, reproduced below.

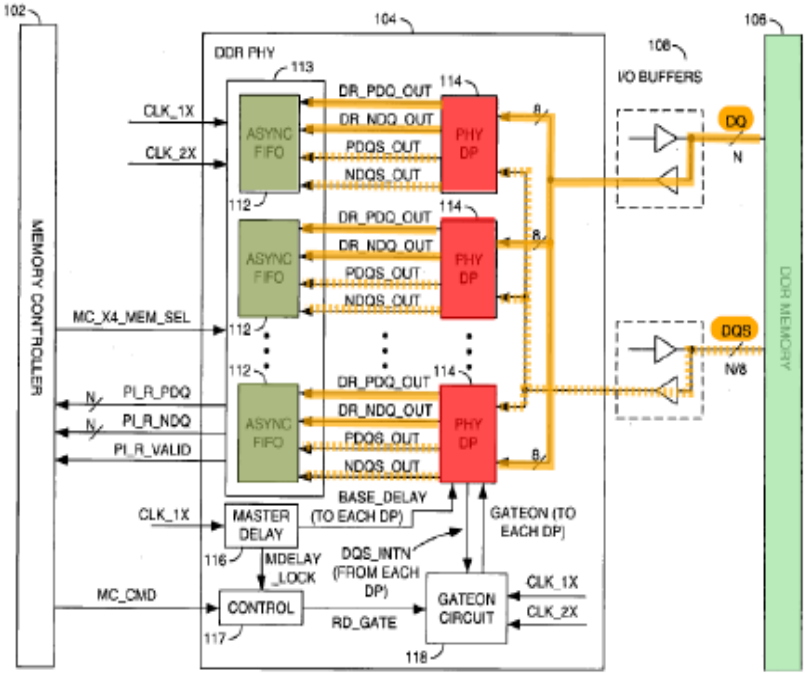

FIG. 2

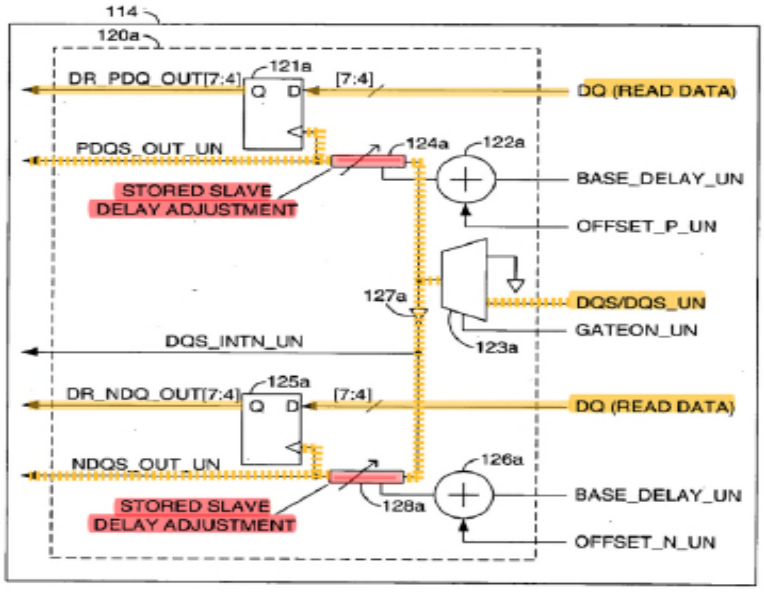

FIG. 3A

Figures 2 and 3A of Butt, above, depict a "datapath," with element 114 of Figure 2 depicting a physical read datapath ("PHY DP") and Figure 3A

depicting a more detailed block diagram of datapath 114. Ex. 1029 ¶¶ 17, 25. Dr. Wedig provides supporting testimony (Ex. 1003 ¶ 144), referring to Butt's disclosure that:

> Each of the physical read datapaths 114 may be configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal or signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal (e.g., GATEON) from the programmable gating signal generator 118. Each of the physical read datapaths 114 may communicate with a corresponding one of the asynchronous FIFOs 112 via a number of signals (e.g., DR_PDQ_OUT, DR_NDQ_OUT, PDQS_OUT, and NDQS_OUT).").

Ex. 1029 ¶ 17 (quoted in Ex. 1003 ¶ 144 (emphasis omitted)).

Petitioner asserts that one of ordinary skill in the art "would have understood from the disclosure of Butt that Hiraishi's data register buffer 300 includes 'data paths' (orange) where data strobe signals sample the data and the data samples are buffered in respective FIFO circuits." *Id.* at 36 (citing Ex. 1003 ¶ 144; Ex. 1029 ¶ 17).

Additionally, Petitioner asserts that Hiraishi discloses a command processing circuit, i.e., "Data Register Control Circuit 320 and logic in DLL Circuit 310," configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal. Pet. 37 (citing Ex. 1003 ¶ 148).

At this stage, Patent Owner presents no arguments specifically related to the merits of the arguments and evidence presented in the Petition as to limitation 1[d]. *See generally* Prelim. Resp. We note that Petitioner has identified portions of Hiraishi that includes portions of data and data strobe signal lines as part of the claimed "data path," as shown in annotated Figure 5 above. Petitioner presents additional evidence and argument based on Butt

as to why a person of ordinary skill in the art would view the portions of Hiraishi that Petitioner relies upon teaches the "data path" as claimed. We invite additional briefing on this issue.

We have reviewed the evidence and argument, which includes unrebutted expert testimony, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that the combination of Hiraishi and Butt teaches limitation 1[d].

vii. Limitation 1[f]

Petitioner asserts that Hiraishi discloses that the data path corresponding to each data signal line includes at least one tristate buffer, i.e. "output buffers OUTB and input buffers INB," controlled by the command processing circuit, and a delay circuit, i.e., "DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376," configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. Pet. 39. Although Petitioner asserts that it is ambiguous as to whether the claim 1 language "in response to at least one of the module control signals" modifies the term "to delay" or the term "determined," Petitioner contends that the combination of Hiraishi and Butt discloses either interpretation. *Id*. at 43 (citing Ex. 1003 ¶ 155).

Petitioner also argues that Hiraishi discloses, with respect to the flow chart shown in Figure 13, a step "S4 Read/Write leveling to determine the delay through the data path." Pet. 42 (citing Ex. 1003 ¶ 152; Ex. 1005, Figs. 5, 13). Petitioner asserts that in a write leveling operation that is "performed during initialization in response to module control signals,"

where "[t]he write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW" such that "the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other," "as shown in Figure 14B." *Id.* at 44–45 (quoting Ex. 1005 ¶¶ 145–146). Then, according to Petitioner, "data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 and performs a re-timing in synchronization with the phase-adjusted internal clock LCLKW which is used to read the FIFO circuit 301 to output the write data DQ and to generate the corresponding strobe DQS with Delay and Strobe Generating Circuits 370 and 374." *Id.* at 46 (citing Ex. 1003 ¶ 161; Ex. 1005 ¶¶ 84, 87, 91, 135, Fig. 5).

Petitioner additionally asserts, for write leveling operations, the alleged "delay circuit" includes

> Write FIFO 301 delaying the write data signal, delay circuit 370 delaying the LCLKW signal, the strobe generating circuit 374 generating a delayed strobe signal that is in synch with the delayed write data, and DLL circuit 310 generating the LCLKW signal for timing the output of the delayed data and strobe signals.

Pet. 47 (citing Ex. 1003 ¶ 161). Petitioner presents similar assertions with respect to the alleged "delay circuit" for read leveling operations, namely, that it includes

> FIFO (read) circuit 302 delaying the read data signal, delay circuit 372 delaying the input strobe signal, the strobe generating circuit 376 generating a delayed strobe signal that is in synch with the delayed read data, and DLL circuit 310 generating the LCLKR signal for timing the output of the delayed read data and strobe signals.

Id. at 51 (citing Ex. 1003 ¶ 166).

At this stage, Patent Owner presents no arguments specifically related to the merits of the arguments and evidence presented in the Petition as to limitation 1[f]. *See generally* Prelim. Resp. We note that Petitioner has identified portions of Hiraishi as the claimed "delay circuit," as discussed above. Our understanding of the claim language, at this juncture, is that the "data path" includes the "delay circuit." We invite additional briefing on this issue.

We have reviewed the evidence and argument, which includes unrebutted expert testimony, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that the combination of Hiraishi and Butt teaches limitation 1[f].

b. Claim 2–5

Petitioner presents evidence and argument in support of its contentions that claims 2–5 would have been obvious over the combination of Hiraishi and Butt. Pet. 53–59. We have reviewed the Petition's showing for these claims and find that sufficient evidence has been provided in support of the challenges at this stage of the proceeding. At this stage, Patent Owner does not contest those claims separately at this juncture. *See generally* Prelim. Resp.

Accordingly, we are persuaded that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that the subject matter of claims 2–5 would have been obvious over the combination of Hiraishi and Butt.

E. Additional Grounds

Petitioner contends that claims 1–5 would have been obvious over the combination of Hiraishi, Butt, and Tokuhiro and claim 5 would have been

obvious over Hiraishi, Butt, and Ellsberry with or without Tokuhiro. Pet. 72–109. At this stage, we find that Petitioner's showing as to obviousness under the first ground is sufficient for institution, and the other grounds will be addressed at trial.

IV. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing at least one of claims 1–5 of the '608 patent is unpatentable under 35 U.S.C. § 103.

V. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–5 of the '608 patent on the grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

IPR2023-00847
Patent 10,268,608 B2

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